WHAT IS CLAIMED IS:

1. A power supply, comprising:

a data signal processing circuit energized by an output supply for producing a data signal, said data signal having a bit-error that is determined by said output supply;

a bit error detector responsive to said data signal for generating a signal indicative of a magnitude of said bit-error in said data signal; and

a power supply regulator coupled to a source of an input supply for generating said output supply and for regulating a magnitude of said output supply in a feedback manner, in response to said bit-error magnitude indicative signal.

2. A power supply according to Claim 1, wherein said data signal contains one of a video information signal and an audio information signal.

3. A power supply according to Claim 1, wherein when said bit-error magnitude is lower than a first threshold value, said output supply magnitude is reduced, in a feedback manner, to a lower magnitude, in which said bit-error magnitude is higher than said first threshold value.

4. A power supply according to Claim 1, wherein said bit error detector generates a signal indicative of a magnitude of a bit-error rate in said data signal.

5. A power supply according to Claim 1, wherein a change in said magnitude of said output supply is established in successive steps.

6. A power supply according to Claim 5, wherein said power supply selectively operates in a normal, run mode of operation and in a standby mode of operation and wherein said

successive steps are performed, outside said normal, run mode of operation.

7. A power supply according to Claim 1, wherein said data signal processing circuit processes a direct-broadcast-satellite input signal of a direct-broadcast-satellite receiver system.

8. A power supply according to Claim 7, wherein said direct-broadcast-satellite receiver system further includes, an antenna coupled to a low-noise block converter for producing said data signal, and wherein said bit-error has a value that is a function of said magnitude of a power-supply voltage which energizes said low-noise block converter.

9. A power supply according to Claim 8, wherein a set of signals received by said antenna comprises a first sub-set of left-hand circularly polarized signals and a second sub-set of right-hand circularly polarized signals.

10. A digital receiver system, comprising:

a power supply for energizing said receiver system with a value of energization;

first means responsive to a signal received by said receiver system for deriving a measurable system-performance value that is a function of said value of energization; and

second means coupled to said power supply and responsive to said measurable system-performance value for reducing said value of energization to that certain value at which said measurable system-performance value is at least an acceptable system-performance value which is below a maximum system-performance value.

11. The digital receiver system defined in Claim 10, wherein said digital receiver system is a direct-broadcast-satellite receiver system.

12. The digital receiver system defined in Claim 11, wherein said second means includes an antenna and a low-noise block converter having a given output response to a given set of signals received by said antenna that have been transmitted from at least one satellite transponder, wherein said given output response is a function of the value of a power-supply-derived voltage which energizes said low-noise block converter and wherein said first means in response to an output signal from said low-noise block converter derives a feedback signal that defines a bit-error-rate-status value that constitutes said measurable system-performance value.